REMARKS

Claims 1-4, 6-15 and 17-20 remain in this application. Claims 1, 6, 7 and 15 have been amended. Claims 5 and 16 have been cancelled. Claims 1, 9 and 15 are independent claims.

In an Office action dated February 24, 2005, claims 9-20 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Takinosawa. Claims 1-8 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Takinosawa in view of Lesea. Applicant firstly requests reconsideration of the finality of the rejection, for reasons to be set forth fully below. Applicant secondly requests reconsideration of the claims in view of the amendments to claims 1, 6, 7 and 15.

Claim 1 has been amended to incorporate the features of claim 5 as originally filed. In order to more particularly point out and distinctly claim the subject matter considered to be the invention, the test bus is identified in claim 1 as being dedicated to providing signaling for the enablement of detecting performance characteristics of individual SERDESs. Claims 6 and 7 have been amended to change their dependency from cancelled claim 5 to amended claim 1. Claim 15 has been amended to incorporate the features of claim 16 as originally filed.

A. The Propriety of the Finality of the Rejection

Applicant respectfully requests that the finality of the rejection be withdrawn because the prematureness of the final rejection has denied Applicant the full opportunity to amend the claims for the purpose of traversing the grounds of rejection, including the new grounds of rejection.

It is well settled that the burden of establishing a *prima facie* case of anticipation or obviousness falls upon the examiner, so that evidence upon which the examiner relies must clearly indicate that the worker of ordinary skill in the art would find the claimed invention to be unpatentable. Ex parte Wolters & Kuypers, 214 USPQ 735 (P.O.Bd.Ap. 1979). In the original Office action (mailed July 27, 2004), it was asserted that Takinosawa teaches all of the features of claim 15. Independent claim 15 describes a method of testing operations of SERDESs of an integrated circuit, including embedding a plurality of test interfaces within the integrated circuit such that each test interface is specific to one SERDES with respect to exchanging parallel data. The method also includes embedding test controllers within the

integrated circuit such that each test controller is specific to one test interface with respect to triggering test operations. In responding to the original rejection of claim 15, claim 15 was not amended. Rather, it was respectfully pointed out that the cited prior art did not teach either of the two "embedding" steps of claim 15.

In the current Office action, the rejection of claim 15 under 35 U.S.C. 102(e) is maintained. However, the rejection of the claim accurately notes that Takinosawa teaches a plurality of test interfaces and test controllers on a plurality of chips, rather than on a single substrate. In the final three lines on page 6 of the current Office action, it is pointed out that Takinosawa discloses the possibility of conducting self tests on two chips. Equally importantly, in addressing Applicant's previously filed remarks, there is no disagreement regarding the lack of a *prima facie* case of anticipation. On page 4 of the Office action, it is submitted that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate" features taught by Takinosawa on the same integrated circuit, in view of a 1965 case decision (i.e., In re Larson, 144 USPQ 347 (CCPA 1965)). However, more recent decisions have discredited the use of such "rules of patentability." For example, in In re Yates, 211 USPQ 1149 (CCPA 1981), the Court reversed a decision of unpatentability when the Solicitor relied upon a 1955 case in order to satisfy the requirement of presenting a *prima facie* case of obviousness. The Court held that the problem with such rules of patentability and their ever-lengthening list of exceptions is that "they tend to becloud the ultimate legal issue - - obviousness - - and exalt the formal exercise of squeezing new factual situations into pre-established pigeonholes."

Since Takinosawa teaches that multiple integrated circuit chips are to be employed if multiple SERDESs and multiple test controllers are to be used in cooperation, the patent publication clearly does not establish a *prima facie* case of anticipation. Moreover, since there is no cited teaching in Takinosawa to modify the prior art method to more closely approach the invention described in claim 15 as originally filed, Takinosawa does not present a *prima facie* case of obviousness under Section 103(a). Because claim 15 was not previously amended, and because the current amendment merely merges the features of claim 16 into claim 15, it is submitted that it is improper to use Lesea in rejecting the claim, unless the finality of the rejection is removed. Applicant respectfully requests that the finality be removed.

B. Rejection of Independent Claim 9

Claim 9 was rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Takinosawa. Claim 9 describes an integrated circuit comprising a single semiconductor substrate onto which integrated circuitry is fabricated. A plurality of SERDESs are integrated onto the substrate, a plurality of functional test interfaces are integrally formed with the substrate, a plurality of functional test controllers are integrally formed with the substrate, and an input/output controller is integrally formed with the substrate. In the Section 102 rejection of the claim, the teachings of Takinosawa are interpreted to teach a substrate having a single "functional test controller" 36 and a single "functional test interface" 35 for performing tests on a single SERDES.

Since Takinosawa does not disclose an integrated circuit having a plurality of SERDESs, a plurality of functional test interfaces, and a plurality of functional test controllers, the prior art reference does not anticipate Applicant's claimed invention. Moreover, in the absence of Applicant's disclosure, there is no motivation within the teachings of Takinosawa to provide an integrated circuit having a plurality of SERDESs, a plurality of functional interfaces, and a plurality of functional test controllers. The closest relevant teaching is found in paragraph [0048] on page 6 of Takinosawa. In this paragraph, it is stated that the various components may be duplicated, but on separate integrated circuit chips. If a cable is used to interconnect the two chips, a transmitter section of one chip and a receiver section of the other chip may be verified. Then, the process is reversed to verify the operation of the other transmitter section and the other receiver section. There is no suggestion in paragraph [0048] or any other portion of Takinosawa to instead incorporate the two transmitter sections and the two receiver sections onto the same chip and to provide different functional test interfaces and different functional test controllers for the two SERDESs that then would be on a single chip.

In addressing Applicant's prior filed remarks, no teaching of Takinosawa was cited for providing a motivation for disregarding the teachings of paragraph [0048] in the patent and instead integrate the various components onto a single semiconductor substrate. Rather, In re Larson was cited for teaching a particular "rule of patentability." As previously pointed out, the holding of the 1965 case and the rules of patentability in general have been discredited in more recent decisions (e.g., In re Yates, 211 USPQ 1149 (CCPA 1981)).

Additionally, it is respectfully noted that even if one were to duplicate the various components of Takinosawa onto a single semiconductor substrate, the resulting integrated circuit would be significantly different than set forth in the pending claim. In the rejection of claim 15, the "input/output controller (IOC)" is identified as the USB link layer 16 of Takinosawa. This USB link layer is the transmitter section of the SERDES. Therefore, duplicating the SERDES necessarily requires duplication of the USB link layer 16. In contrast, claim 9 describes the input/output controller (IOC) as being "connected to each said FTC to transmit individually addressed commands to each said FTC." Thus, while claim 9 describes an IOC connected to each functional test controller, the modification of the teachings of Takinosawa proposed in the Office action would include a separate IOC for each "functional test controller."

While Lesea was not cited in the Office action with respect to claim 9, Applicant submits that even if one were to modify the teachings of Takinosawa in view of Lesea, the resulting integrated circuit would not render claim 9 obvious under Section 103. In referring to Lesea on page 10 of the current Office action, Fig. 1 is cited for showing a plurality of SERDESs integrated onto a substrate. If one were to modify the teachings of Takinosawa to include multiple SERDESs onto a single substrate, there would be an equal number of IOCs (i.e., USB link layers 16). Since the combination of teachings does not present a *prima facie* case of obviousness, Applicant asserts that claim 1 and its dependent claims are patentably distinguished from the teachings of Takinosawa and Lesea, whether taken separately or in combination.

Reconsideration of claim 9 and its dependent claims is requested.

C. Rejection of Independent Claim 15

As previously noted, claim 15 has been amended to incorporate the features of claim 16 as originally filed. Therefore, the patentability of amended claim 15 will be considered in view of the rejections of claims 15 and 16.

Claim 15 describes a method of testing operations of SERDESs of an integrated circuit, with the method including embedding a plurality of test interfaces and embedding a plurality of test controllers within the integrated circuit. The method also includes providing an integrated circuit output that

enables the test controllers to be individually addressed and includes embedding an input/output controller (IOC) so that the IOC is connected between the integrated circuit output and the test bus to which each test controller is linked.

In rejecting claim 15, the current Office action correctly points out that Takinosawa discloses that it is possible to conduct self test on two chips. The testing of two chips is described in paragraph [0048] on page 6 of the patent publication. Then, in the rejection of claim 16, it is stated that Takinosawa teaches that data to be transmitted is provided by the micro controller 12 to the "input/output controller" (i.e., the USB link layer 16). Since the USB link layer 16 is an integral part of the SERDES, duplication of the SERDES necessarily results in duplication of the "input/output controller." In claim 15, the method includes providing the integrated circuit output that enables test controllers to be individually addressed and includes connecting the input/output controller between this integrated circuit output and a test bus. Such connectivity is not described in Takinosawa, even if one were to duplicate the circuitry of Takinosawa as suggested in the Office action.

Fig. 1 of the pending application shows one possible implementation of the invention. In this implementation, the input/output controller 38 is connected between the test bus 36 and the integrated circuit output (SERIAL PORT). Because amended claim 15 describes each test controller being linked to the test bus and describes the input/output controller as being between the test bus and the integrated circuit output, the input/output controller cannot be an integral part of the SERDES. Therefore, the USB link layer 16 of Takinosawa does not teach or suggest the input/output controller of amended claim 15.

While Lesea was not cited for teaching the obviousness of the combination of claims 15 and 16, Applicant respectfully points out that the connectivity resulting from the method described in amended claim 15 is not suggested in Lesea, even if combined with the features Takinosawa. It follows that the combination of prior art references does not present a *prima facie* case of obviousness with respect to the amended claim.

Reconsideration of claim 15 and its remaining dependent claims is requested.

D. Rejection of Independent Claim 1

Claim 1 has been amended to describe each tester as being connected to a common test bus and to describe each tester as having a unique address that enables independent accessibility of the tester via the test bus. The test bus is dedicated to providing signaling for the enablement of detecting performance characteristics of the individual SERDESs.

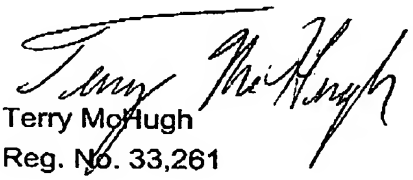
The amendment to claim 1 incorporates the features of claim 5 as originally filed. Specifically, the description of the test bus was incorporated from original claim 5. In the rejection of claim 5, the Office action states that Takinosawa teaches "the USB link layer 16 (core processing logic) functions to provide data to be transmitted in a parallel form (e.g., 16 bit word) to the USB physical layer 18 (SERDESs) via a data bus 21 (common test bus)." Unlike the rejections of independent claims 9 and 15, it is agreed that Takinosawa does not teach incorporating a plurality of SERDESs onto a single substrate. Page 2 of the Office action states:

> The Applicant rightfully relates the USB physical layer 18 comprises a built-in self-test (TX-BIST) circuit 35, a multiplexer 36 and a built-in self-analyzer circuit 49 to the tester circuit within the SERDES. However, it was not the Examiner's intention to identify these components as the "plurality of testers", but when the USB physical layer is repeated (i.e. the two USB physical layers on page 6, ¶ 48) it became a "plurality of testers". Since the built-in self-test (TX-BIST) circuit 35, multiplexer 36 and built-in self-analyzer circuit 49 is part of a single SERDES circuit or USB physical layer 18 it would stand to reason that these components comprise a single tester circuit.

Since Takinosawa does not teach a plurality of SERDESs or a plurality of testers on a single substrate, there is no teaching or suggestion that testers should be connected to a common test bus or that each of a plurality of testers should have a unique address that enables independent accessibility of the tester via the test bus. Lesea was not cited for teaching this feature. Moreover, amended claim 1 states that the test bus is dedicated to providing signaling for the enablement of detecting performance of characteristics of the individual SERDESs. A dedicated test bus is not taught or suggested by the cited prior art, even when combined as suggested in the Office action.

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicant invites the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,



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